

2
3 ATHERMAL ANNEALING WITH RAPID THERMAL ANNEALING SYSTEM AND METHOD

4
5 BACKGROUND

6 (1) Field

7 The disclosed methods and systems relate generally to
8 annealing processes, and more particularly to athermal annealing.

9 (2) Description of Relevant Art

10 Conventional ion implantation systems include ionizing a
11 dopant material such as boron, accelerating the ions to form an
12 ion beam having a given energy level, and directing the ion beam
13 energy at a semiconductor surface or wafer to introduce the
14 dopant material to the semiconductor and alter the conductivity
15 properties of the semiconductor. Once the ions are embedded into
16 the crystalline lattice of the semiconductor, the ions can be
17 activated using a process known as rapid thermal annealing (RTA)
18 or rapid thermal process (RTP). During RTA, the semiconductor
19 can be introduced to a furnace to heat the semiconductor at a
20 prescribed temperature and for a prescribed time. RTA can also
21 cure defects in the crystalline structure that can be caused by
22 the ion implantation.

23 The processes of ion implantation and RTP contribute to the
24 depth of the implanted region, known as the junction depth.

Those of ordinary skill in the art recognize that the junction depth from ion implantation is based on the energy of the ions implanted into the semiconductor. Accordingly, shallow implanted regions can be formed using low-energy ion beams. Unfortunately, traditional methods of RTA include raising the temperature of the silicon to ranges nearing 1100-1200 degrees Celsius, which can approach the melting temperature of the silicon. Accordingly, RTA can further increase the implanted junction depth as high temperatures of the RTA process cause further diffusion of the implanted region.

The increase in junction depth can be particularly troublesome when considered with respect to a continuing and expanding demand for smaller devices, and hence shallower junction depths. It is anticipated that the present methods and systems that combine ion implantation solely with traditional RTA may not satisfy the demand for shallower junctions.

SUMMARY

The disclosed methods and systems include features for annealing a semiconductor structure that include subjecting the semiconductor structure to an oscillating magnetic field and applying a low temperature rapid thermal annealing (LRTA) process to the semiconductor structure. The electromagnetic field can be a time-varying electromagnetic field that can be

1 provided by, for example, a signal having a frequency in the
2 microwave or the radio frequency (RF) bands.

3 In one embodiment, the LTRTA can include exposing the
4 semiconductor to a temperature less than approximately 800
5 degrees Celsius, while in another embodiment, the temperature can
6 be greater than approximately 500 degrees Celsius, and less than
7 approximately 800 degrees Celsius. The RTA can be performed in a
8 furnace or another annealing device.

9 For the disclosed methods and systems, the LTRTA can be
10 performed either before or after the application of
11 electromagnetic field or energy.

12 The methods and systems can accordingly be implemented with
13 and/or applied to ion implantation systems where dopant material
14 ions can be implanted into a semiconductor structure or wafer.
15 The semiconductor wafer can include silicon or Gallium Arsenide,
16 for example. The dopant can be any one of an n-type dopant and a
17 p-type dopant.

18 Other objects and advantages will become apparent
19 hereinafter in view of the specification and drawings.
20

21 BRIEF DESCRIPTION OF THE DRAWINGS

22 FIG. 1 is one embodiment of a system and method for
23 performing Electromagnetic Induction Heating (EMIH) annealing
24 using microwave frequencies;

1 FIG. 2A is a TM011 magnetic field pattern;
2 FIG. 2B is a TM111 magnetic field pattern;
3 FIG. 3 is one embodiment of a radio frequency system and
4 method for performing EMIH annealing;
5 FIG. 4 displays a relationship between power absorption and
6 conductivity;
7 FIG. 5 displays a relationship between conductivity and
8 temperature for various dopant levels;
9 FIG. 6 includes a SEMATECH barrier curve for evaluating
10 improvements in anneal and doping technology; and,
11 FIG. 7 provides a SIMS profile for as-implanted and
12 microwave spike annealed plasma doped (PLAD) samples.

14 DESCRIPTION

15 To provide an overall understanding, certain illustrative
16 embodiments will now be described; however, it will be understood
17 by one of ordinary skill in the art that the systems and methods
18 described herein can be adapted and modified to provide systems
19 and methods for other suitable applications and that other
20 additions and modifications can be made without departing from
21 the scope of the systems and methods described herein.

22 Unless otherwise specified, the illustrated embodiments can
23 be understood as providing exemplary features of varying detail
24 of certain embodiments, and therefore features, components,

1 modules, and/or aspects of the illustrations can be otherwise
2 combined, separated, interchanged, and/or rearranged without
3 departing from the disclosed systems or methods.

4 During ion implantation, the implanted regions can be
5 damaged when the accelerated, energized dopant ions collide with
6 the host or silicon surface, displacing silicon atoms from their
7 original lattice sites. Although the dopant ions can be in high-
8 energy non-equilibrium positions in the silicon lattice, the
9 dopant ions are not electrically active. A rapid thermal
10 annealing (RTA) process can provide energy to the silicon and
11 dopant ions to allow movement of the ions to equilibrium
12 positions, thereby also repairing the implantation damage by
13 restoring crystallographic order. Unfortunately, the RTA process
14 that exposes the semiconductor surface to high temperatures in
15 the range of 1000-1200 degrees Celsius, often also causes dopant
16 redistribution or diffusion. RTA for certain implant doses can
17 increase junction depths to be significantly deeper than, for
18 example, the as-implanted range.

19 For example, with regard to transistor devices, the
20 consequences of a continued demand for small devices can be
21 anticipated to include a limiting of lateral diffusion under the
22 gate and a maintenance of high concentration of dopant material
23 in a shallow source/drain extension region. Accordingly, the
24 disclosed methods and systems include a combination of athermal

annealing and rapid thermal annealing (RTA) to obtain a very shallow junction with a device having a low sheet resistance. The methods and systems accordingly utilize electromagnetic fields to induce current flow through a silicon wafer and cause ohmic collisions between high energy electrons and the silicon lattice structure to provide rapid heating of the silicon from within the structure, as opposed to RTA that applies high temperatures to the structure surface. The athermal heating of the silicon, referred to herein as Electromagnetic Induction Heating (EMIH), provides energy to activate the dopant that can provide greater activation than a method or system using RTA (also referred to and known as RTP). Low temperature RTA (LTRTA), understood herein to be temperatures less than approximately 800 degrees Celsius, but for the illustrated embodiments, preferably between approximately 500 degrees Celsius and approximately 800 degrees Celsius, can also be performed before and/or after the EMIH to further repair the silicon structure and minimize diffusion. LTRTA can be performed at a temperature, and for a time period, that can be significantly less than generally associated with processes that only use RTA annealing for dopant activation and crystallographic defect curing. Those of ordinary skill in the art recognize that merely using LTRTA can fail to activate the dopant and hence can result in a large sheet resistance. Accordingly, by combining the

1 athermal annealing to provide dopant activation and the LTRTA
2 (approximately 500-800 degrees Celsius) RTA to cure the
3 structural defects, the dopant material can be activated, the
4 lattice structure can be repaired, and differences between the
5 as-implanted junction depth and the post-annealing junction depth
6 can be minimized when compared to methods that use only RTA.

7 EMIH can be understood as a unique application of Faraday's
8 and Ampere's laws. As a silicon wafer is exposed to oscillating
9 magnetic fields, electrons are induced to flow within the wafer.

10 As the electrons collide with the lattice, they release energy
11 that heats the silicon wafer. This athermal, internal heating
12 via EMIH can be compared to, for example, RTA that generally
13 exposes the wafer to a furnace at a prescribed temperature and
14 causes the silicon to be heated from the outside surface in,
15 thereby raising a possibility of silicon melt.

16 Those with ordinary skill in the art recognize that for
17 highly conducting materials such as copper, induced currents re-
18 induce a magnetic field that partially or completely interferes
19 with the incident electromagnetic field. Alternately, insulating
20 materials such as quartz lack free carriers and hence preclude
21 any flow of current, thereby allowing the incident field to
22 penetrate the material. Semiconductors such as silicon can have
23 properties of conductors and insulators, and thus can have a

1 potential for significant electromagnetic field penetration that
2 can induce substantial currents throughout the wafer volume.

3 In the disclosed methods and systems, electromagnetic fields
4 can be induced by subjecting the silicon sample to
5 electromagnetic energy having frequencies in the radio frequency
6 (RF) and microwave ranges, although those with ordinary skill in
7 the art will recognize that the methods and systems are not
8 limited to these frequency ranges, and other methods of inducing
9 electromagnetic energy can be used. The rapid, internal ohmic
10 heating of the wafers caused by the induced currents in the
11 silicon wafer can cause dopant activation that can be more
12 effective than the activation that can be caused by the surface
13 heating provided by RTA.

14 Referring now to FIG. 1, there is one embodiment of a
15 microwave system that includes a resonant cavity having a radius
16 of seventeen centimeters, and a height that can be adjusted
17 between fifteen and forty-five centimeters for tuning to specific
18 microwave modes. A magnetron source can provide a maximum three
19 thousand watts of power at 2.45GHz. One of ordinary skill in the
20 art will recognize that various modes can be provided by a system
21 according to FIG. 1, including but not limited to the well-known
22 TM011 and TM111 modes. FIGs. 2A and 2B provide magnetic field
23 patterns in the FIG. 1 microwave cavity for the TM011 and TM111
24 modes, respectively.

1 Referring to FIG. 3, there is a RF embodiment of the
2 disclosed methods and systems that utilizes an exciting RF
3 magnetic flux with a spiral copper antenna. A power supply
4 matched through an L-type matching network can provide up to one-
5 thousand Watts at a fixed 13.56MHz frequency. In the FIG. 3
6 system, a silicon wafer can be positioned on a ceramic chuck two-
7 and-a-half centimeters below the coil windings in an extreme near
8 field of the antenna. In the illustrated system, the ceramic
9 chuck can be heated to one-hundred fifty degrees Celsius.

10 Those with ordinary skill in the art will recognize that the
11 exemplary electromagnetic induction systems of FIGs. 1 and 3 are
12 merely illustrative and the implementation thereof is not limited
13 to the embodiments or characteristics provided herein.
14 Furthermore, although FIGs. 2A and 2B provide two magnetic field
15 patterns, such patterns are provided for illustration and not
16 limitation. Accordingly, other systems that utilize alternate
17 methods, frequencies, apparatus, magnetic field patterns, fewer
18 or additional components or alternatives, etc., can be used
19 without departing from the scope of the methods and systems
20 disclosed herein.

21 For the illustrated systems of FIGs. 1 and 3, temperature
22 measurements can be provided by collecting radiated light using
23 an optical pyrometer or light pipe. The collected radiated light
24 can be analyzed by, for example, a Luxtron model analyzer that

1 matches the collected light intensities to a block body radiation
2 spectrum to produce a temperature of the silicon wafer. In some
3 embodiments, the spectrum may be modified or scaled to provide an
4 accurate temperature measurement based on the emissivity of
5 silicon.

6 The EMIH methods and systems can allow a prediction of a
7 magnitude of the induced currents, and hence, the temperature.
8 As provided previously herein, a solution of Faraday's and
9 Ampere's laws can provide a description of the induced current
10 density and the power absorbed, where:

$$11 \quad P_{ABS} = \frac{\pi a^2 t_w^3 / (\delta^4 \sigma)}{1 + (t_w / \delta)^4} H_0^2, \quad \delta = \sqrt{2 / \omega \mu \sigma} \quad (1)$$

12 where δ is skin depth, ω is frequency, μ is permeability, σ is
13 conductivity, t_w is thickness, "a" is radius, and H_0 is the
14 incident magnetic field. FIG. 4 provides a plot of power
15 absorption based on conductivity according to Equation 1. As
16 FIG. 4 and Equation 1 indicate, the absorbed power increases with
17 conductivity, σ , until a peak absorption is reached. Thereafter,
18 the absorbed power decreases at the same rate of the increase and
19 asymptotes to zero.

20 The relationship between temperature and conductivity can be
21 instrumental to understanding the FIG. 4 relationship between
22 power absorption and conductivity. FIG. 5 provides the
23 relationship between conductivity and temperature for a variety
24 of substrate doping levels. It is well-known that although

conductivity can be expressed as a product of mobility and carrier density, mobility decreases with temperature due to an increased collision frequency that impedes carrier flow, while carrier density increases with temperature as the increased thermal energy moves carriers from the valence band to the conduction band. Accordingly, as FIG. 5 indicates, conductivity can decrease until the temperature exceeds approximately one-hundred degrees Celsius, during which time collisions impede carrier mobility. As the temperature further increases, the increase in intrinsic carriers can exceed the loss in mobility to allow the conductivity to monotonically increase with temperature. The largest conductivity illustrated in FIG. 5 relates to the peak power absorption level in FIG. 4, and accordingly, when viewing FIGs. 4 and 5 together as a function of increasing temperature, it can be seen that for the smaller illustrated levels of doping, as temperature increases to approximately one-hundred degrees Celsius, conductivity (FIG. 5) decreases and hence power absorption (FIG. 4) is also decreasing, thereby preventing the wafer temperature from increasing. This can otherwise be known as an absorption valley. As the wafer temperature increases beyond this temperature (FIG. 5), however, conductivity increases with temperature, thereby also causing an increase in power absorption (FIG. 4) that can cause a rapid increase in temperature. At approximately five-hundred degrees

1 Celsius, the intrinsic carrier concentration can greatly exceed
2 the doping such that the conductivity, and hence heating, becomes
3 independent of the substrate doping, and silicon wafers of
4 varying dopant dosages can heat with identical characteristics.

5 Based on FIG. 4 and 5, and the inference that higher
6 frequency fields (e.g., microwave) can heat more efficiently than
7 lower frequency fields (e.g., RF), in some embodiments, it can be
8 necessary to pre-heat the silicon wafer to a temperature above
9 the absorption valley. In some embodiments, for given power
10 levels, the same wafer temperature can be achieved irrespective
11 of whether one or more wafers are present. Accordingly, batch
12 processing can be equally as effective.

13 In one embodiment of the methods and systems, B^+ and BF_2^+
14 ions, at a dose of $10^{15}/cm^3$, were implanted into n-type silicon
15 wafers having resistivities between 10 and 20 ohm-cm over a range
16 of implant energies between 250 eV and 2.2keV. Another sample
17 was implanted at a dose of $10^{15}/cm^2$ using plasma doping (PLAD)
18 (BF_3 gas). The samples were annealed using EMIH, and
19 specifically RF and microwave embodiments, to either 900 or 1000
20 degrees Celcius in an uncontrolled ambient at atmospheric
21 pressure. FIG. 6 illustrates sheet resistances versus junction
22 depth evaluated at $10^{18}/cm^3$ from SIMS. The solid line in FIG. 6
23 is the present SEMATECH barrier curve for evaluating improvements
24 in anneal and doping technology. Those of ordinary skill in the

1 art recognize that data points below the SEMATECH curve indicate
2 a higher percentage of activated dopants and/or a more efficient
3 annealed dopant profile than the SEMATECH standard.

4 Referring now to FIG. 7, there are plots of SIMS results for
5 the as implanted and microwave spike annealed PLAD samples.
6 Those with ordinary skill in the art also recognize that a more
7 efficient profile can be obtained by a controlled ambient of
8 oxygen (e.g. 33 to 100ppm) to eliminate the oxygen-enhanced-
9 diffusion effect.

10 In one embodiment of the methods and systems disclosed
11 herein, sheet resistances were measured for implants of B+ at
12 250eV and 500eV, and BF2+ at 500eV, 1.1keV, 2.2keV, and 4.5keV,
13 with implant doses of $1.0 \times 10^{15}/\text{cm}^2$, using EMIH annealing, and
14 specifically, RF annealing at 13.96 MHz. In some embodiments,
15 the RF anneal time was thirty seconds to 1000 degrees Celsius and
16 900 degrees Celsius, while a spike anneal was applied in other
17 embodiments to the same temperatures. In all measured categories
18 of ion beam energy, the thirty-second, 1000 degree temperature RF
19 annealing provided the best sheet resistance, on the order of
20 nearly 300 ohms/sq. to 850 ohms/sq. The remaining experiments
21 described herein provided sheet resistances on the order of 500
22 ohms/sq to 7000 ohms/sq. Accordingly, although the RF annealing
23 activates the dopant, defects remained in the lattice structure.

1 In another embodiment where microwave EMIH annealing was
2 performed at 2.45GHz, for thirty-second and spike annealing at
3 1000 and 900 degrees Celsius, sheet resistance measurements
4 varied on the order of 150 ohms/sq. to 1000 ohms/sq. Once again,
5 defects remained in the lattice structure.

6 By performing LTRTA (i.e., approximately 500 - 800 degrees
7 Celsius) before or after EMIH annealing, defects in the lattice
8 structure caused by the implantation can be cured without the
9 undesirable diffusion effects caused by traditional RTA methods
10 that necessarily provide silicon temperatures in a range between
11 900 degrees Celsius and 1200 degrees Celsius to activate the
12 dopant. Accordingly, using the disclosed methods and systems
13 that combine EMIH with low-temperature RTA, a junction and
14 structure having high concentration dopant activation and lattice
15 repair with low diffusion and sheet resistance, can be achieved.

16 What has thus been described is a method and system to
17 achieve shallow junctions using Electromagnetic Induction Heating
18 (EMIH) that can be preceded or followed by a low-temperature
19 Rapid Thermal Annealing (RTA) process. The methods and systems
20 can use, for example, RF or microwave frequencies, to induce
21 electromagnetic fields that can induce currents to flow within
22 the silicon wafer, thus causing ohmic collisions between
23 electrons and the lattice structure that heat the wafer
24 volumetrically rather than through the surface. Such EMIH

1 heating can activate the dopant material. Defects in the silicon
2 structure can be repaired by combining the EMIH annealing with a
3 low-temperature (approximately 500 - 800 degrees Celsius) RTA
4 that causes minimal diffusion, thus minimizing the difference
5 between the as-implanted junction depth and the post-annealing
6 junction depth when compared to annealing methods that only use
7 traditional RTA.

8 The methods and systems described herein are not limited to
9 a particular hardware or software configuration, and may find
10 applicability in many computing or processing environments. The
11 methods and systems can be implemented in hardware or software,
12 or a combination of hardware and software. The methods and
13 systems can be implemented in one or more computer programs
14 executing on one or more programmable computers that include a
15 processor, a storage medium readable by the processor (including
16 volatile and non-volatile memory and/or storage elements), one or
17 more input devices, and one or more output devices.

18 Although the methods and systems have been described
19 relative to a specific embodiment thereof, they are not so
20 limited. Obviously many modifications and variations may become
21 apparent in light of the above teachings. For example, although
22 the methods and systems illustrated herein referred to silicon
23 semiconductors, other semiconductors, for example, from group IV
24 of the periodic table, can be used, as well as other

1 semiconductors. Furthermore, although the sample embodiments
2 indicated Boron (B+) as a p-type dopant, the methods and systems
3 can be applied to n-type dopants. Although LTRTA was illustrated
4 as approximately 500-800 degrees Celsius, where the LTRTA can be
5 performed using a furnace, LTRTA can be understood to include an
6 exposure to temperatures less than approximately 800 degrees
7 Celsius. The methods and systems disclosed include providing an
8 oscillating magnetic field to induce the currents in the
9 semiconductor, and although the illustrated methods and systems
10 provided RF and microwave systems, any electromagnetic wave of
11 any frequency that provides a time-varying or oscillating
12 magnetic field can be used. For example, an EMIH embodiment can
13 include a permanent magnet that can be moved to provide a time-
14 varying magnetic field.

15 Many additional changes in the details, materials, and
16 arrangement of parts, herein described and illustrated, can be
17 made by those skilled in the art. Accordingly, it will be
18 understood that the following claims are not to be limited to the
19 embodiments disclosed herein, can include practices otherwise
20 than specifically described, and are to be interpreted as broadly
21 as allowed under the law.